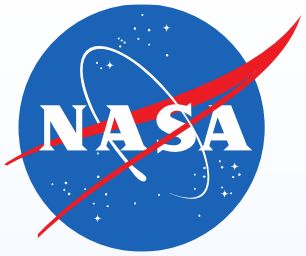

Jet Propulsion Laboratory
California Institute of Technology

Radiation Performance of Memory Technologies for Space Applications

Steven M. Guertin, Jean Yang-Scharlotta, and Raphael Some

steven.m.guertin@jpl.nasa.gov
818-321-5337
NASA/JPL

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Outline

- The need for space memory
- Memory selection approach
- Technology study: commercial devices
- DDR2 study
- MRAM study
- Conclusions

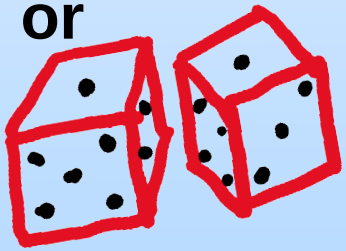
Want to have a memory (or maybe two) to enable high total dose tolerance & without SEFI risk…

Space Memory Study

- **Selection of memory for space mission:**
  - **Reliability (including radiation)**
  - **SWaP**
  - **Application needs**
- **Study reported last year at RADECS pointed out parameters for needed space memory**
  - **Errors limited to SBUs, no SEFIs resulting in more than 1 bit error in a single address**
  - **Need devices with at least 100 krad(Si) survivability**
- **But all current devices have problems**
  - **Chip density is too low**
  - **Cannot provide radiation performance**
  - **Require too much power**

Space Memory Limitations

- **Trade space consists of NVM, high current volatile, and in-betweens**
  - **Generally SRAM is used and can be rad hard, but power usage is very high, and size limited to ~200Mb, requiring ~2W**
  - **DRAMs use about 1W / 3Gb, and coming down**
    - **Have significant SEFI problems**
  - **Flash memory is much lower power, but cannot meet TID requirements**
- **But all current devices are either too small or cannot provide radiation performance**



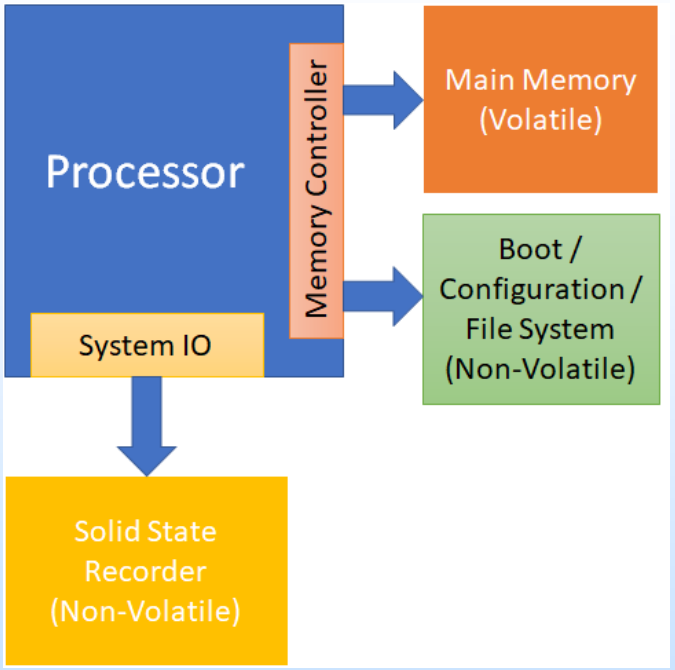
- **Occasionally there is a lucky part, but that is the exception, not the rule.**

Desires for Space Memory

- **Volatile Memory – computer memory**
  - **TID performance of 100-300 krad(Si)**
  - **No need to power cycle or reinitialize – SEFI immune**
  - **No MBU in a single device read**
  - **Support DDR3 interface**
  - **No more than 1W/1Gb**
  - **~512 Mb/device (we would like >1 Gb/device – scalability)**
- **Non-Volatile – data storage**
  - **TID performance of 100-300 krad(Si)**
  - **No SEFI**
  - **Support NAND flash interface (or similar)**
  - **~1W/100Gb**
  - **>512 Mb/device (we would like >4 Gb/device – scalability)**

- **Possible single solution**
  - **If all requirements could be met on a single device**
    - **Some "desires" can be flexed, like lower density if higher is coming**
  - **Probably necessary to compromise on density**

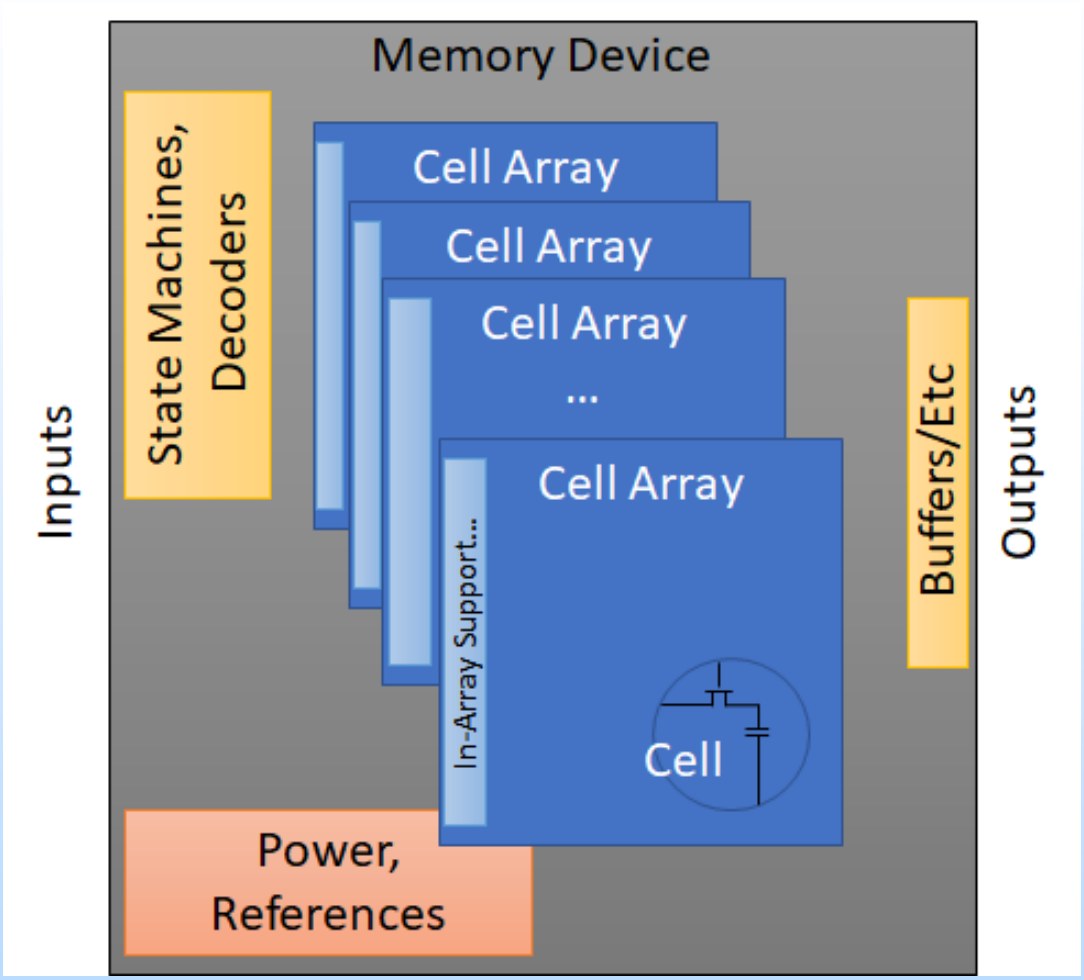
Candidate Technologies



- **Approaches that may work**
  - Identify a memory technology capable of meeting all requirements
  - Partnering with a memory manufacturer
  - Build control circuitry with rad hard elements, mate to viable memory technology (single-chip or stacked)
- **DRAM**
  - Lower than ~1W/1Gb – DDR3 & DDR4
  - (Some) recent devices exceed 300 krad(Si)
- **MRAM**
  - Non-Volatile
  - Lower power than DRAM
  - Lower density, but larger commercial devices are becoming available
- **Excluded:**
  - SRAM (power), Flash (hardness), phase-change (density), etc…
  - But we continue to monitor and test promising technologies

Commercial Devices

- Some commercial manufacturers are interested in providing memory arrays
  - To be mated to rad-hard controllers
- Generally they want to have data collected at the component level, rather than providing test structures
- Testing has been focused on how to test the array within a full commercial device
  - The array may contain local control circuitry that cannot be replaced



Cartoon of memory device structure indicating the "cell array", which may be a repeated structure. If the cell array is robust to radiation effects, it should be possible to build the rest of the circuit in RHBD to provide desired performance.

MRAM Selection

- **Working with MRAM partner**
  - **The bit/memory array is the key**
  - **Tested manufacturer's recommended commercial device**
- **Test plan focus on memory array**
  - **Test unbiased when possible**
    - **Part of larger approach to minimize impact of device-level circuits that can be replaced**
- **Tested for TID, SEE (SBU, MBU, and SEFI), and SEL**
  - **Targeting the program requirements: No SEL under LET 75 MeV-cm^2/mg, TID of 300 krad(Si) or more**
  - **MBU not as critical because it can be masked by controller.**

MRAM SEL, SBU, & TID

- **No SEL - LET of 84 MeV-cm^2/mg, 1×10^7 /cm^2 exposure**

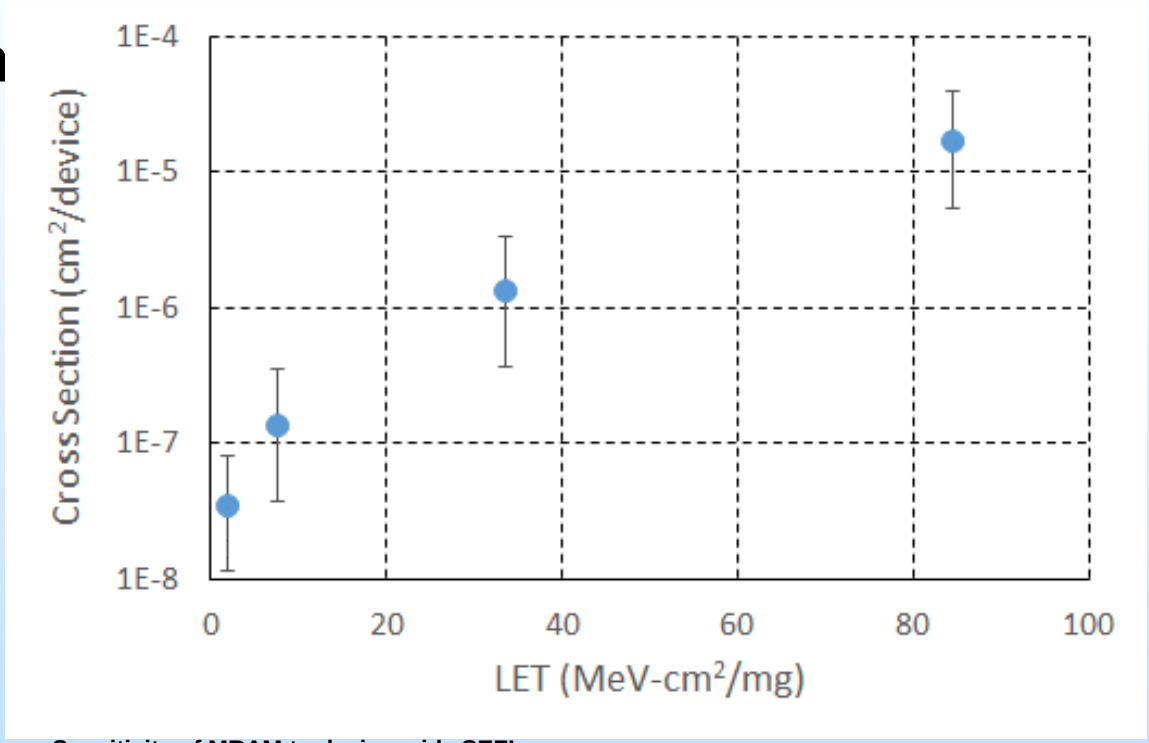
- **No SBU – tested in static mode**
  - **Non-volatile cells could easily be isolated this way**

Ion	Energy	LET	Fluence	Bit Errors
Ne	25 Mev/amu	1.9 MeV-cm2/mg	2.00E+07	0
Ar	25	7.6	2.00E+07	0
Kr	25	33.7	2.00E+07	0

- **No TID errors**
  - **Tested to 50, 100, 200, 300, 400, and 1500 krad(Si)**
  - **Refreshed data on each test**
  - **1.1 Mrad(Si) was largest individual irradiation without refresh**
  - **Single memory-device unbiased no change at 7 Mrad(Si)**
    - **This technology, but not a commercial DUT**

MRAM SEFI

- **One interesting behavior observed in the MRAM test devices was a SEFI that resulted in all data being lost.**
- **This behavior is attributed to the control circuitry and is expected to be possible to mitigate in a production device.**



Sensitivity of MRAM to device-wide SEFI

DDR2 Selection

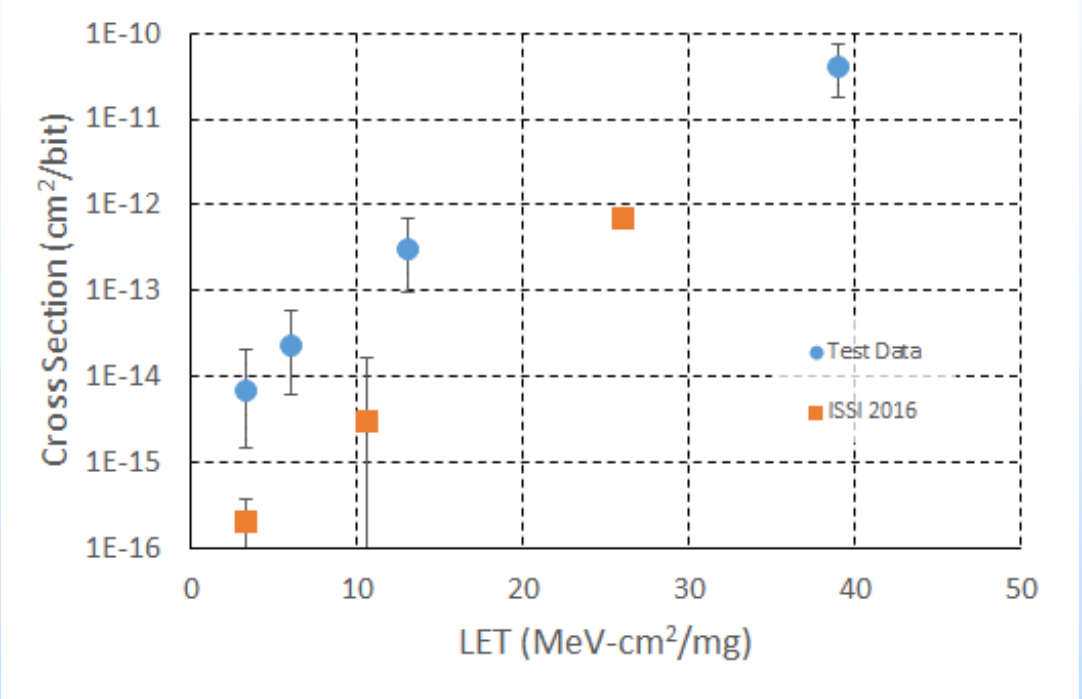
- **Working with DDR2 partner**
  - **The bit/memory array is the target portion**
  - **The manufacturer recommended a specific DDR2 device, but can the memory array is agnostic to the DDR interface**
  - **Tested device is 1 Gb (64M x16) device**
- **TID testing performed (JPL gamma source) on 1 static-biased device, and 1 device that was refreshed**
  - **Refreshed is worst case, but significantly more difficult to perform**
- **SEE testing performed at TAMU**
  - **SEL, SBU, MBU, and SEFI**

DDR2 SEL &TID Results

- No SEL: 1.9V, 95C, using 2×10^7 /cm^2 @ LET 83 MeV-cm^2/mg
- For DDR2, we test at room temperature only, and simulate higher temperature by increasing the refresh period.
- 1s refresh period is similar to ~75C operation
- 4s refresh is similar to 95C
- Only 1 bit was stuck (2 DUTs) at 300 krad(Si)
  - We observed significant changes in # of stuck bits as measurements were made
  - ~100 stuck bits with 4s refresh period
  - Worst-case… if devices were actually heated, stucks anneal
- Note that refreshed devices had ~10x higher stuck bits

DDR2 SBU Sensitivity

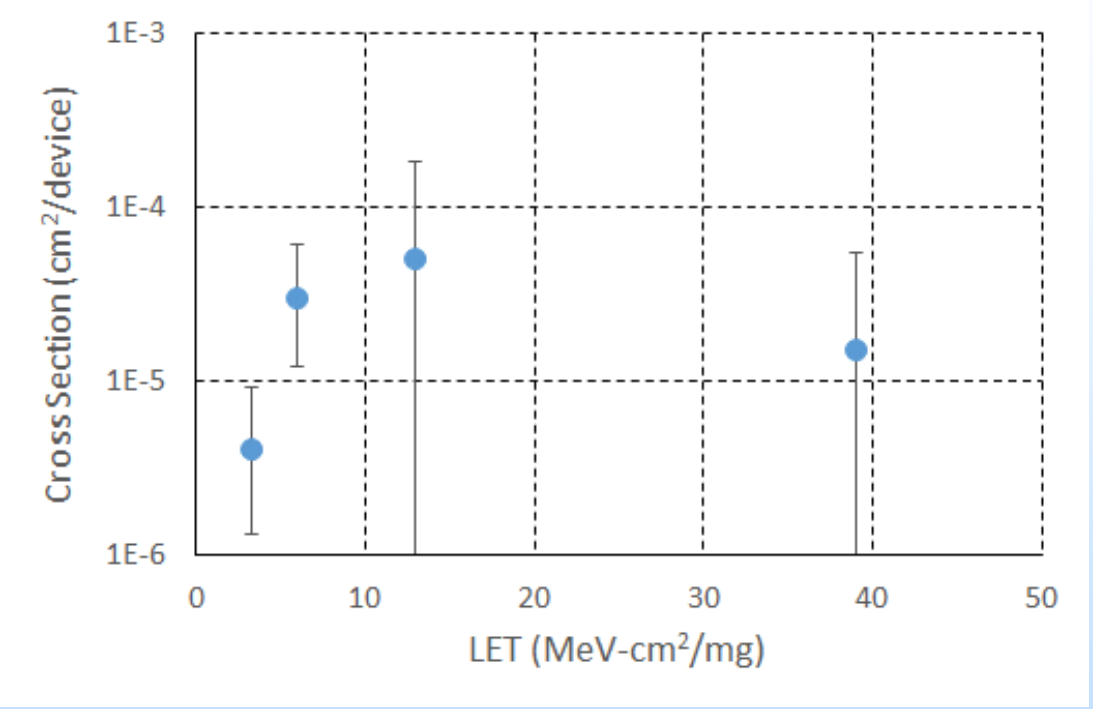
- **Test device exhibited SBUs**
  - **No multiple-bit upsets observed in a single address**
- **Compared to other DDR2 device (ISSI tested in 2016)**
  - **Note this ISSI device is an example of rad-hard by luck**
  - **The tested device is consistent with expected SBU performance**



–Single Bit Upset sensitivity of tested DDR2 device Compared to ISSI DDR2 used in some missions.

DDR2 SEFI Sensitivity

- Tested DDR2 devices showed SEFIs
- Two types of SEFIs (rough)
  - Millions of errors
  - Thousands of errors
- Large SEFIs are the result of the controller
- Small SEFIs may be intrinsic to the cell array
  - (Row SEFI, where all bits on a row are lost)



–DRAM SEFI sensitivity. Note that many SEFIs resulted in the device showing millions of errors.

Conclusions

- There are no viable memories for space systems
  - Implementation is too complex – multiple power planes
  - Radiation performance is insufficient – 300 krad, SEFI
- One approach is to find a memory technology that can meet radiation performance
  - Partner with manufacturer
  - Build a rad-hard device with custom controller
  - We focused on MRAM and DRAM
- MRAM memory array TID results very good, SEE good except for possible device-wide SEFI
  - We infer the memory array is good
- DRAM memory array TID results very good, SEE good but with some SEFIs that are not surprising
  - A memory controller could correct them
  - Some are probably intrinsic to the design and unavoidable
- Future work: increase test samples, additional biased tests

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End